

Title: METHOD OF FABRICATING A
WIRING BOARD UTILIZING A
CONDUCTIVE MEMBER HAVING A
REDUCED THICKNESS

Inventor(s): Akira CHINDA et al.

Appl. No.: 10/684,423



FIG. 1A PRIOR ART

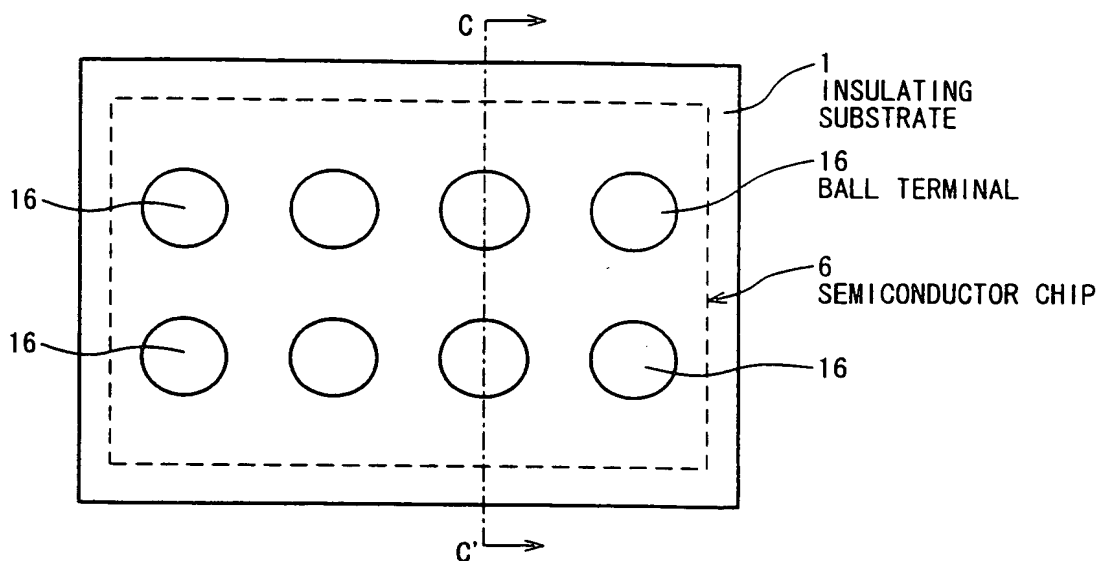
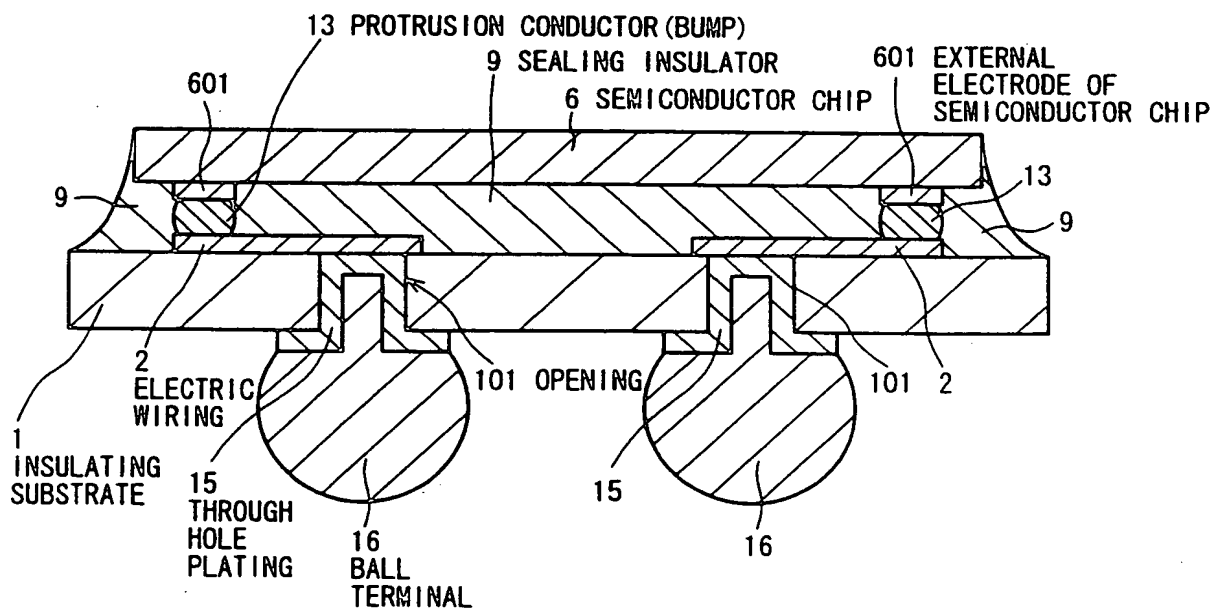


FIG. 1B PRIOR ART

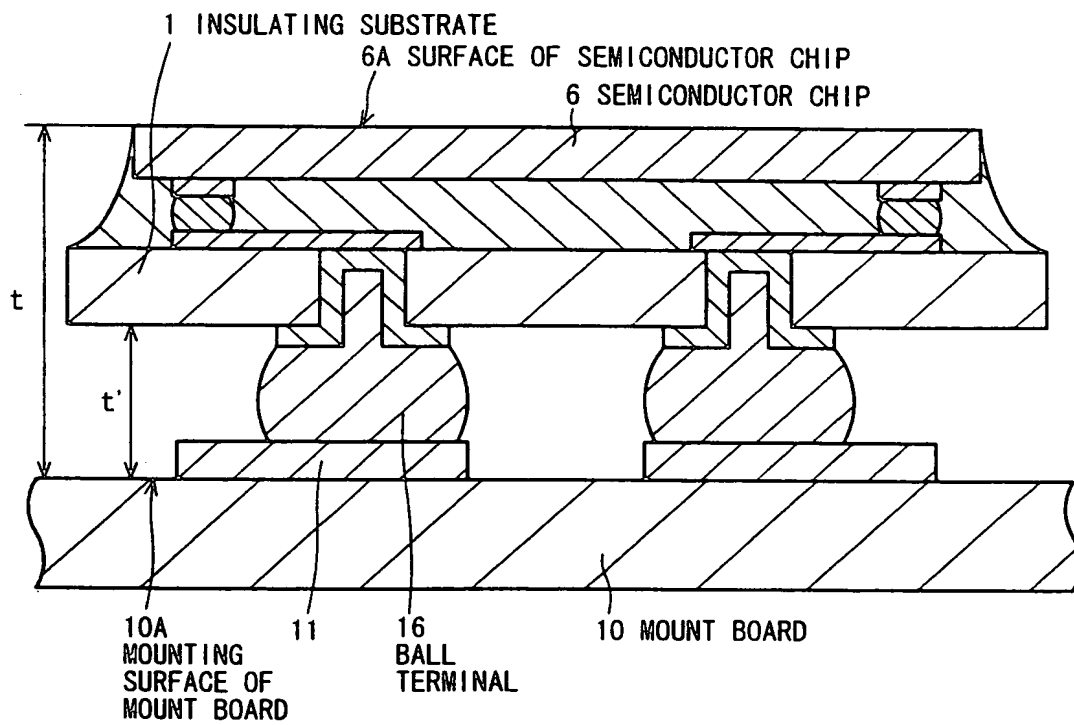


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FIG. 2 PRIOR ART

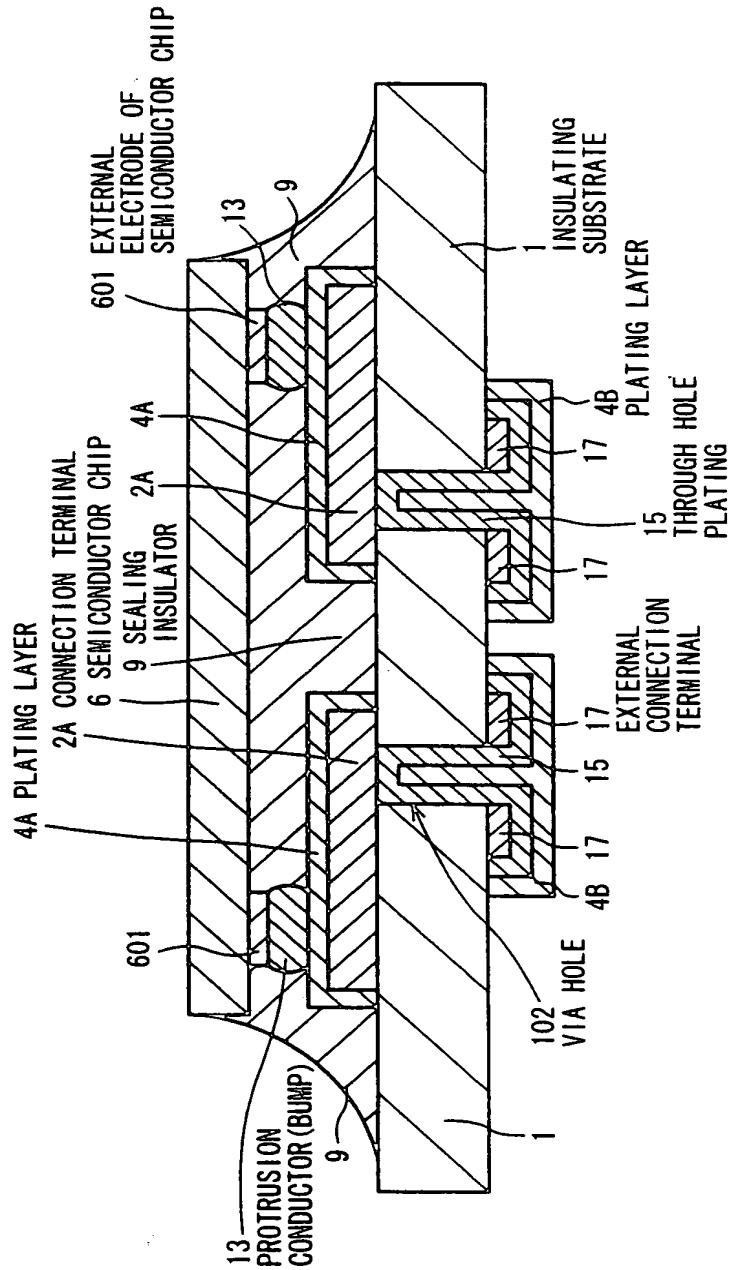


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FIG. 3 PRIOR ART



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FIG. 4A PRIOR ART

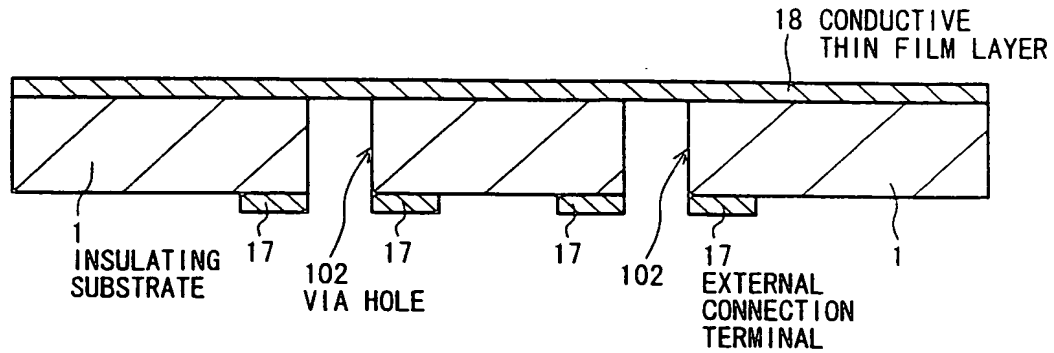


FIG. 4B PRIOR ART

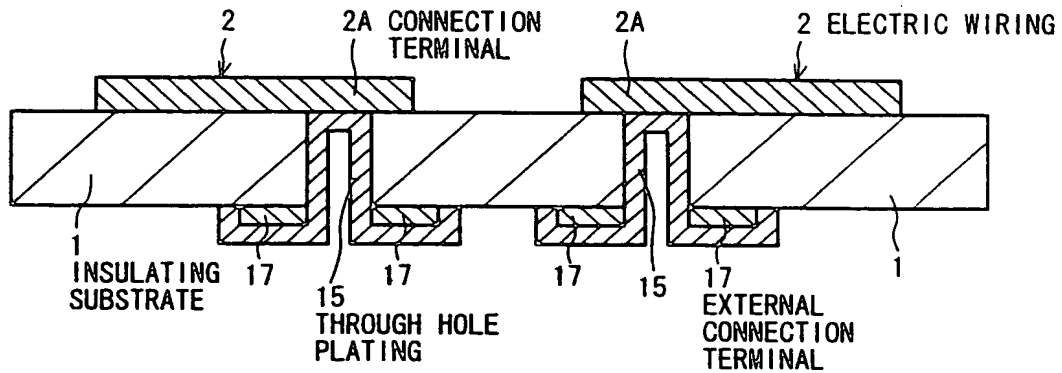
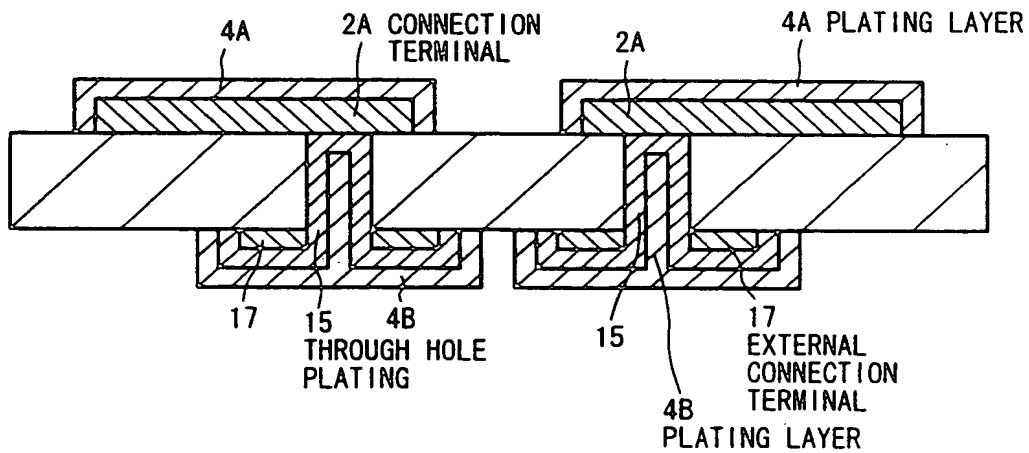
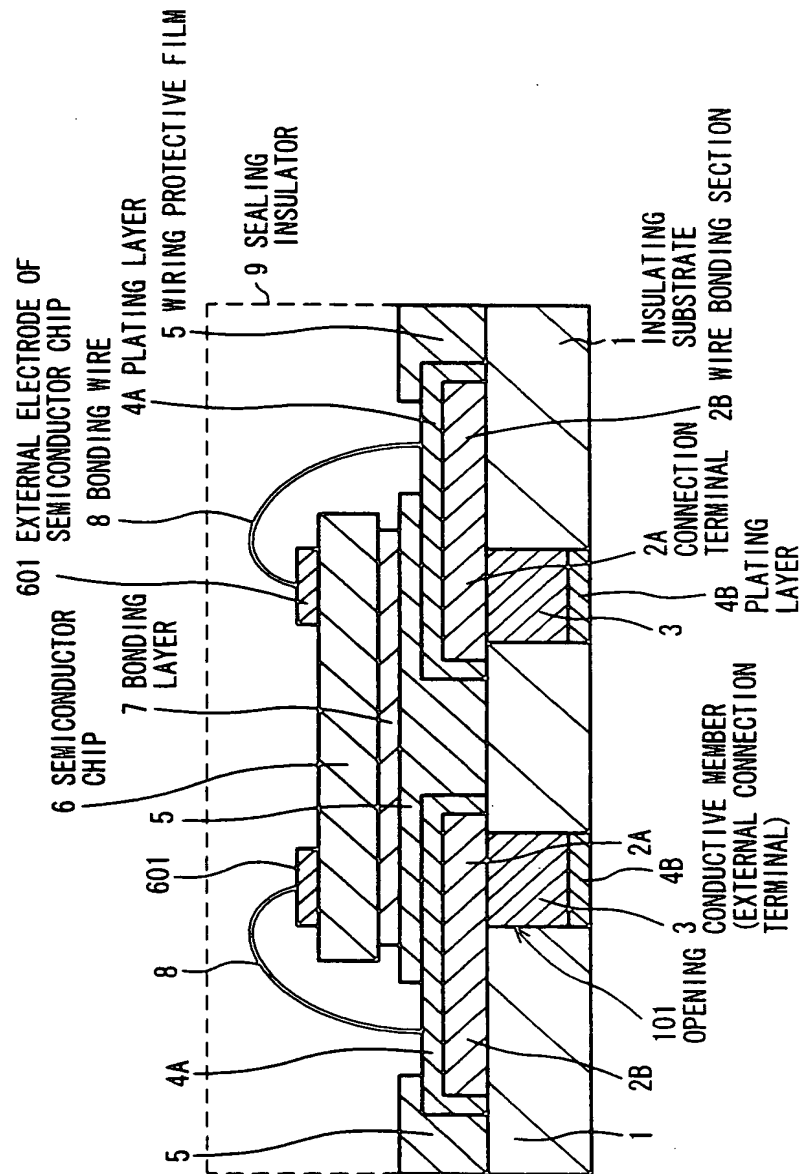


FIG. 4C PRIOR ART



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FIG. 6



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FIG. 7A

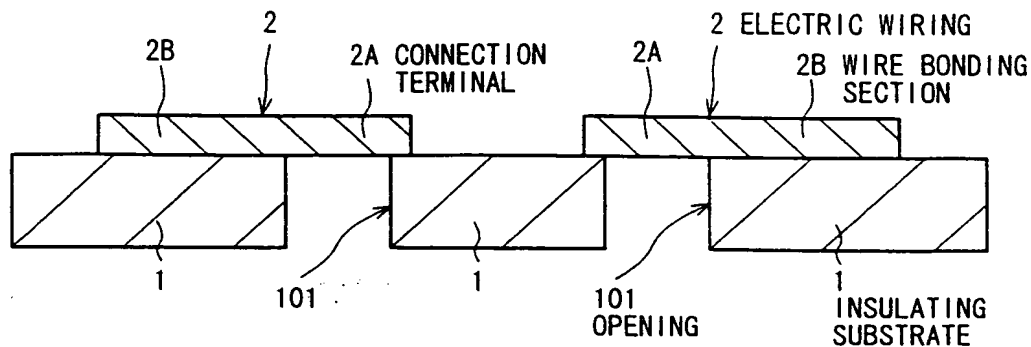


FIG. 7B

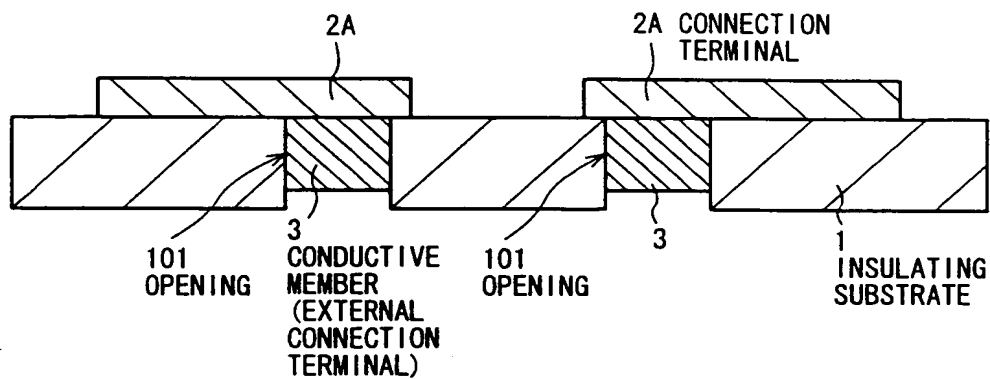


FIG. 7C

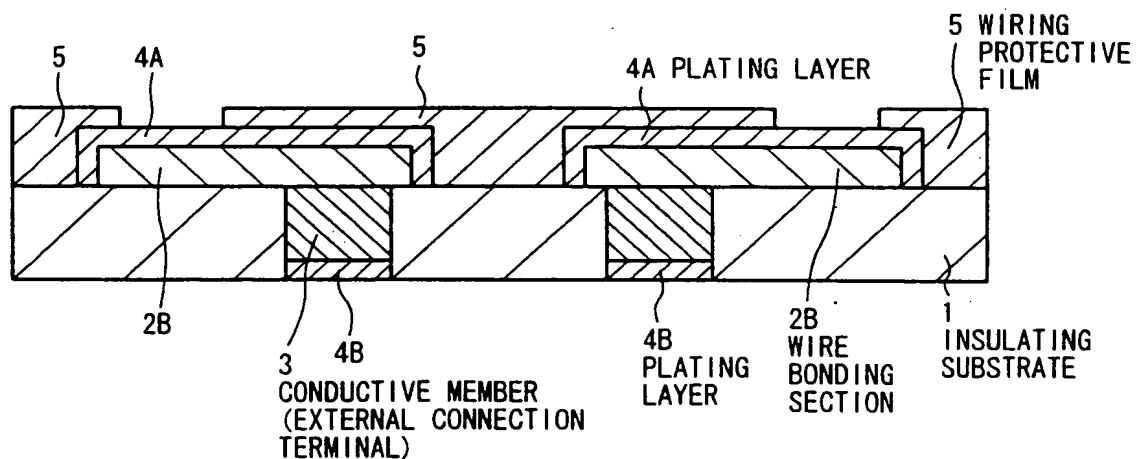


FIG. 8

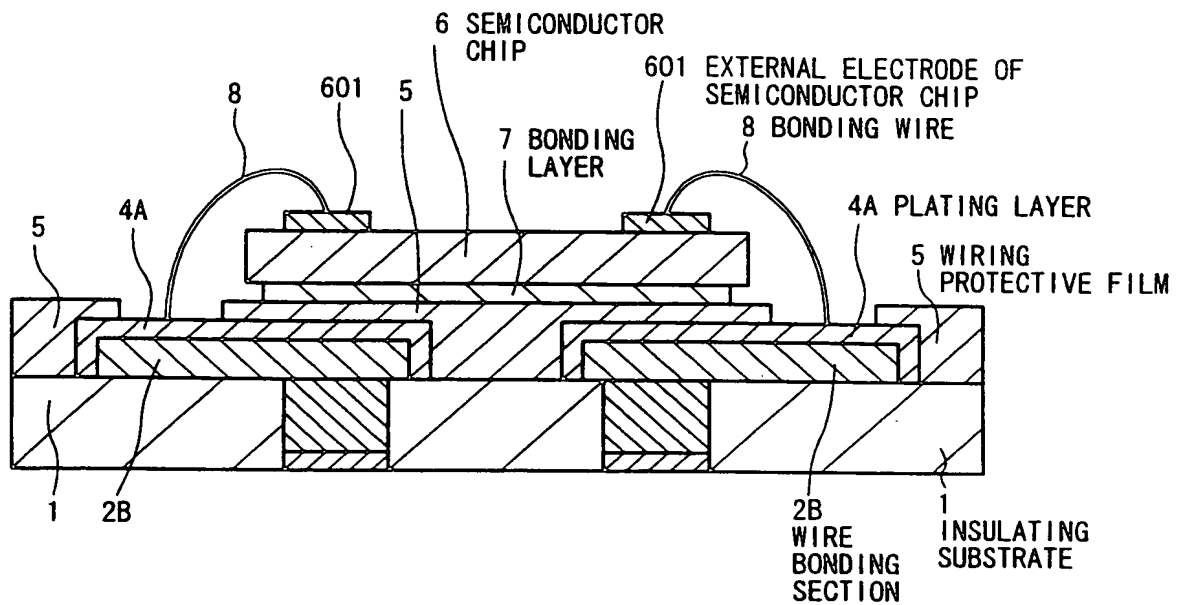
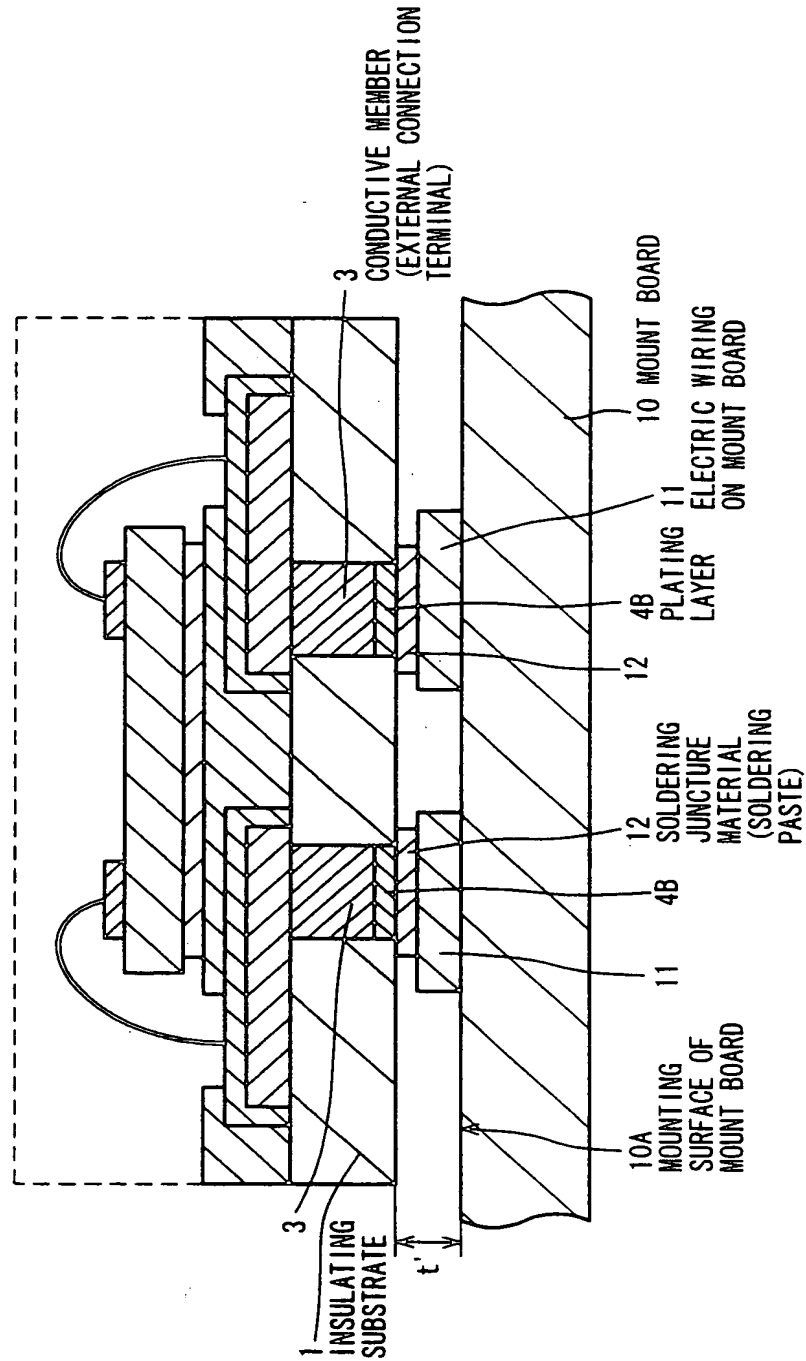


FIG. 9

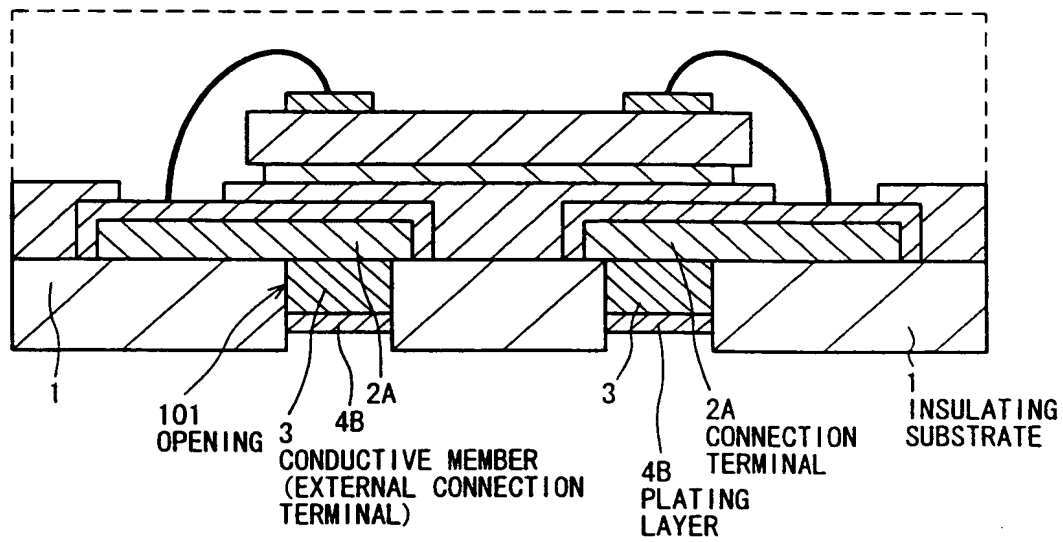


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FIG. 10

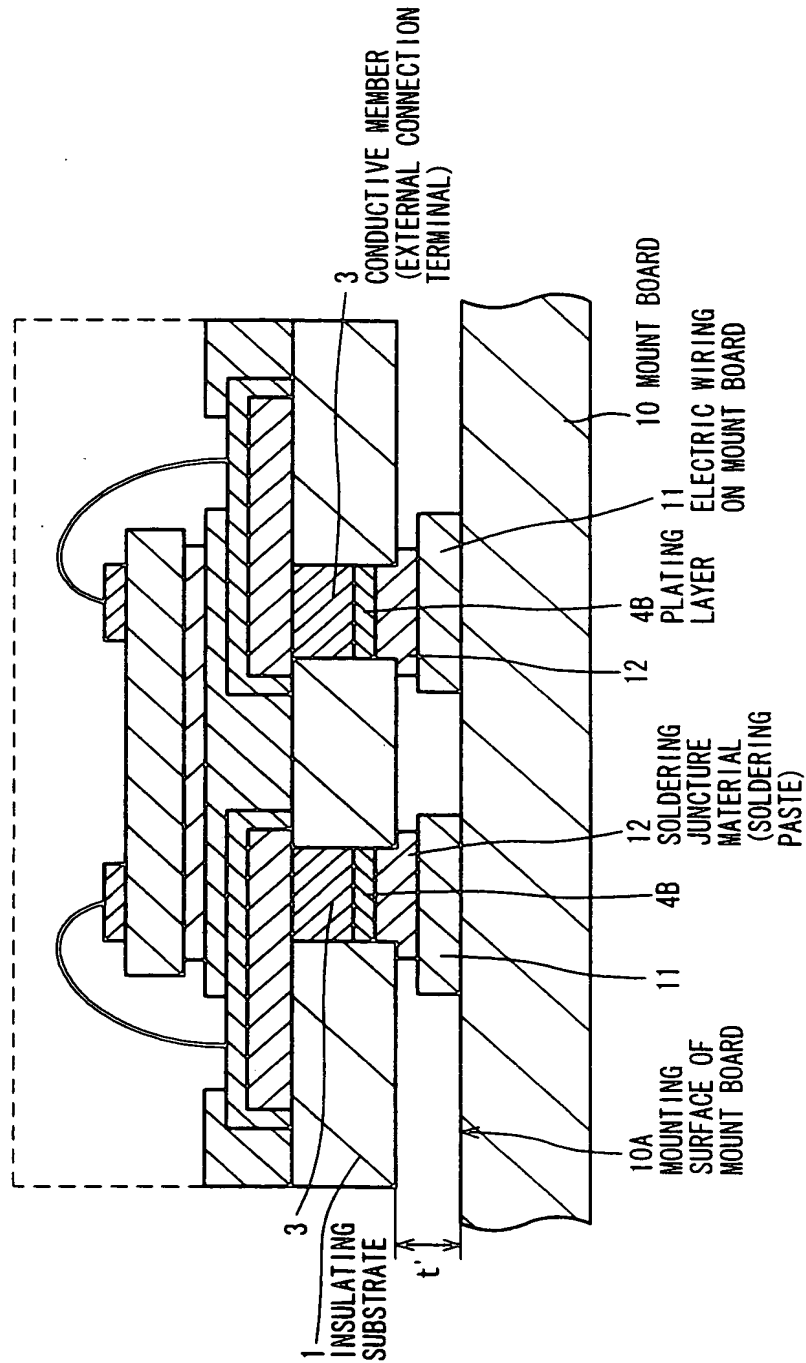


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FIG. 11



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FIG. 12

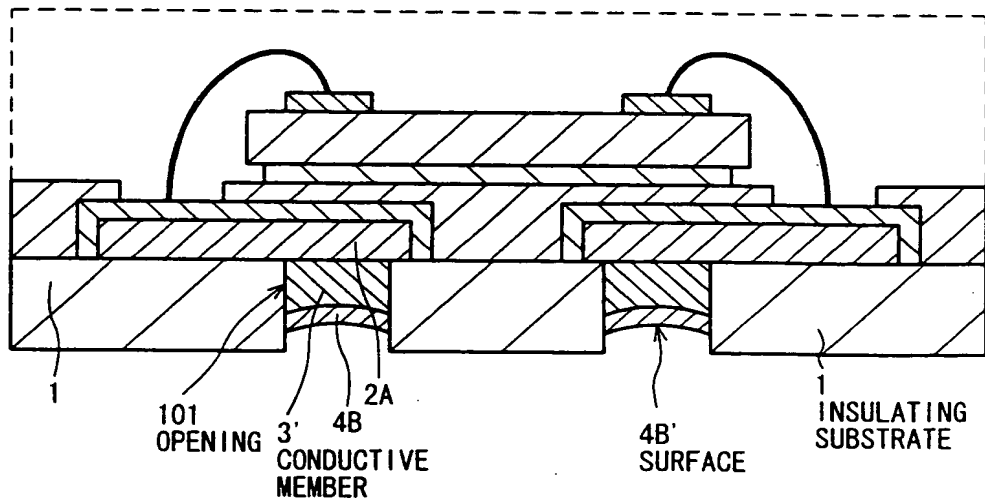
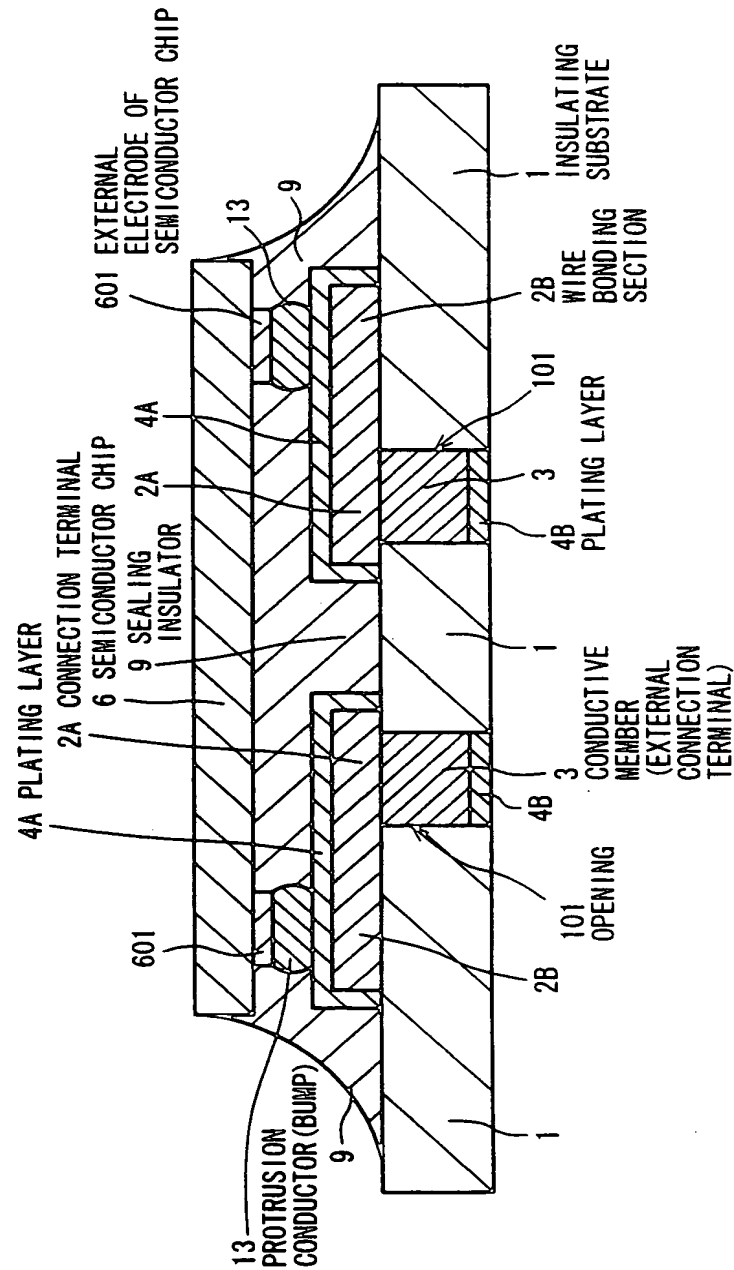


FIG. 1 is a plan view of a semiconductor chip 6. The chip is mounted on an insulating substrate 1. A grid of connection terminals is formed on the chip surface. Each terminal consists of a central conductive member 3 (external connection terminal) surrounded by a plating layer 4B. The terminals are arranged in a grid pattern. The chip is labeled with '6 SEMICONDUCTOR CHIP' and '1 INSULATING SUBSTRATE'. Arrows B and B' indicate directions. Labels for the terminals include: '2B WIRE BONDING SECTION', '2 ELECTRIC WIRING', '2A CONNECTION TERMINAL', '3 CONDUCTIVE MEMBER (EXTERNAL CONNECTION TERMINAL)', '4B PLATING LAYER', '101 OPENING', and '3 CONDUCTIVE MEMBER (EXTERNAL CONNECTION TERMINAL)'.

THE METHOD OF FABRICATING A

FIG. 14

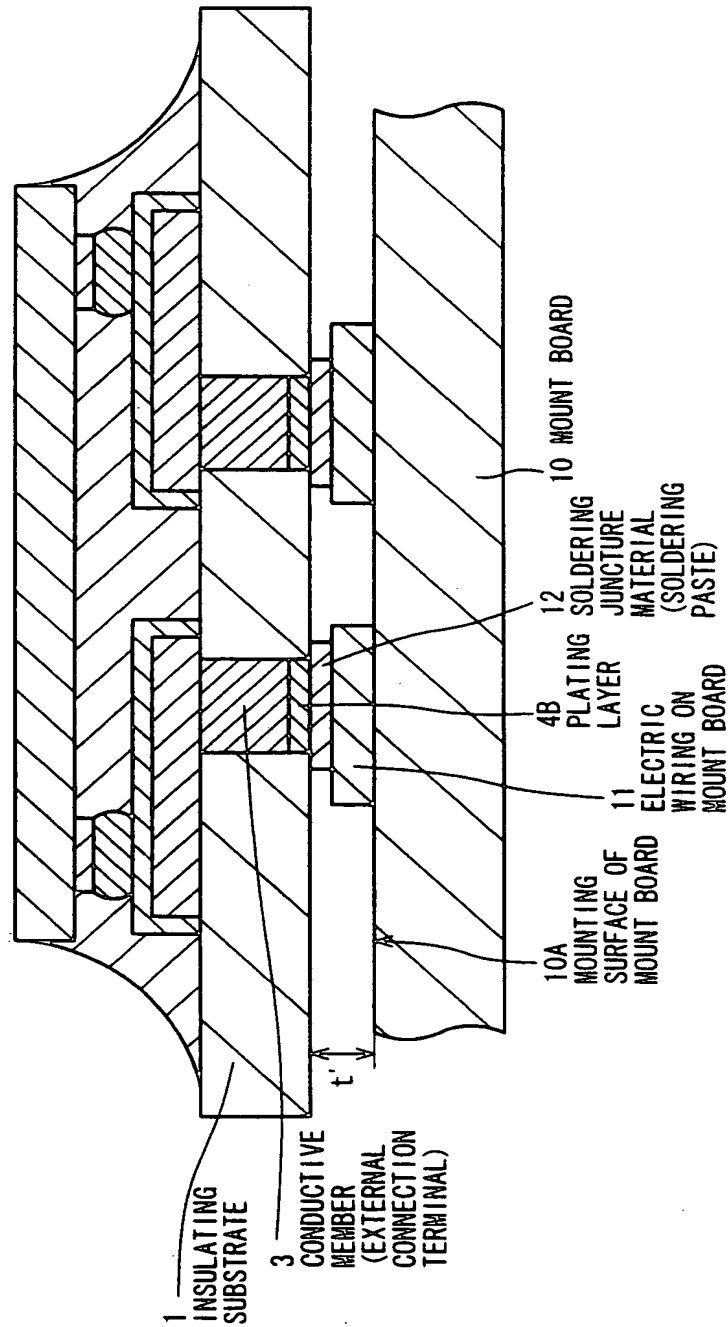


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FIG. 15

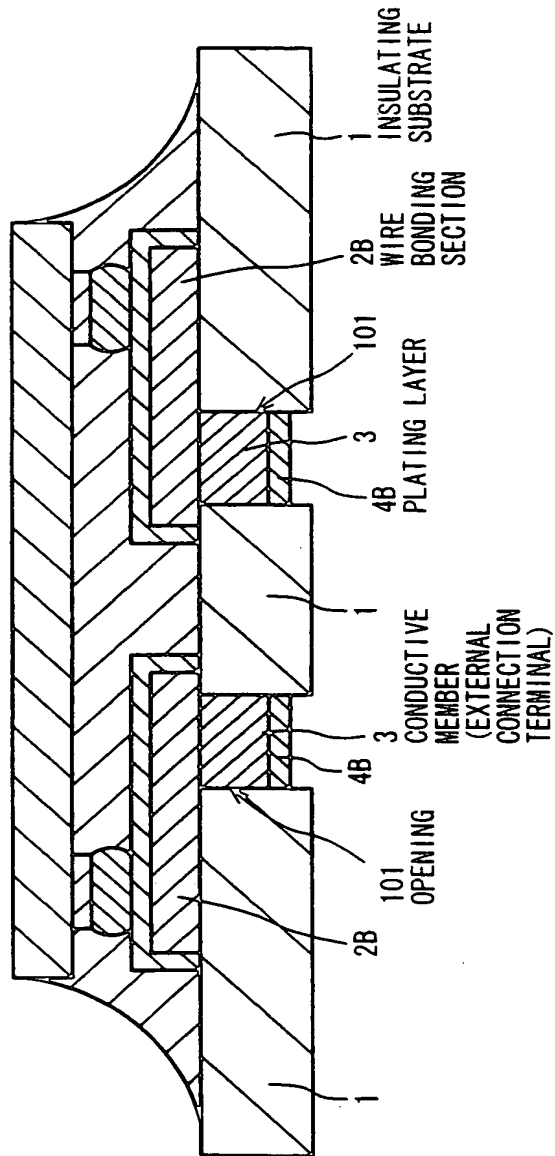


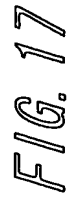
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FIG. 16





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FIG. 18

